

**600V High and Low Side Driver**
**PRODUCT SUMMARY**

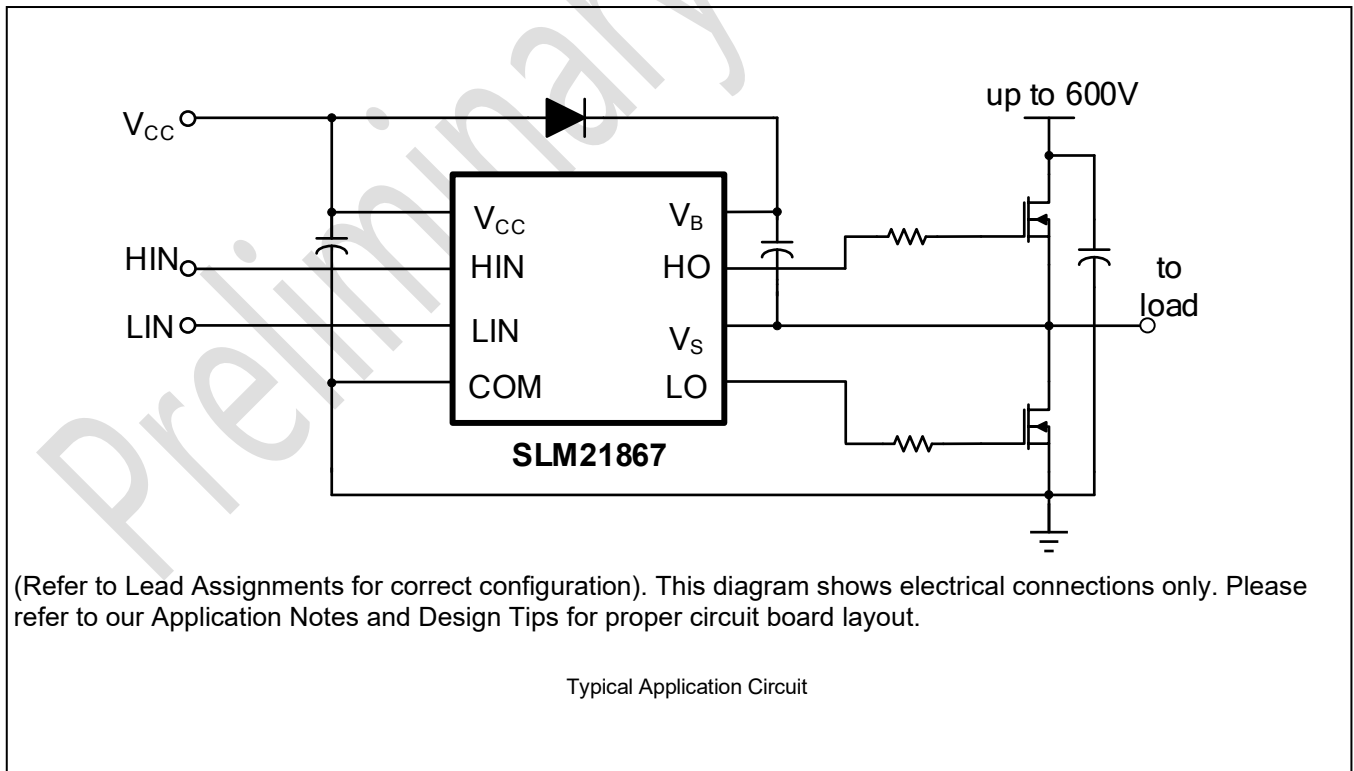
- $V_{\text{OFFSET}}$  600 V max.
- $I_{\text{O}+/-}$  4 A / 4 A
- $V_{\text{OUT}}$  7 V - 20 V
- $t_{\text{on/off}}$  (typ.) 170ns / 170ns

**GENERAL DESCRIPTION**

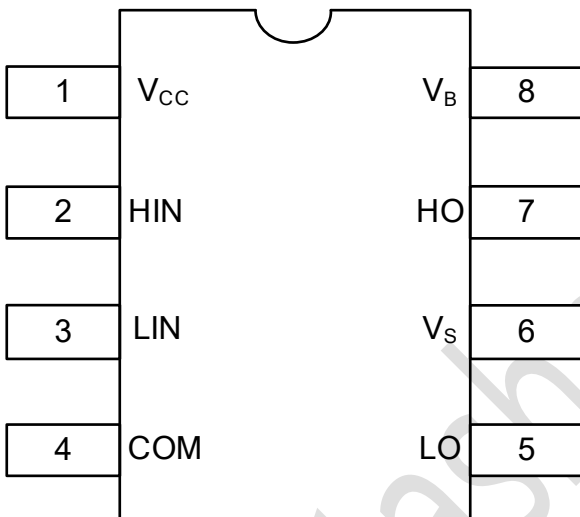
The SLM21867 is a high voltage, high speed power MOSFET and IGBT drivers with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

**FEATURES**

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Low  $V_{\text{CC}}$  operation
- Tolerant to negative transient voltage,  $dV/dt$  immune
- Gate drive supply range from 7 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, and 5 V logic compatible
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant
- SOIC-8 package

**TYPICAL APPLICATION CIRCUIT**


**PIN CONFIGURATION**

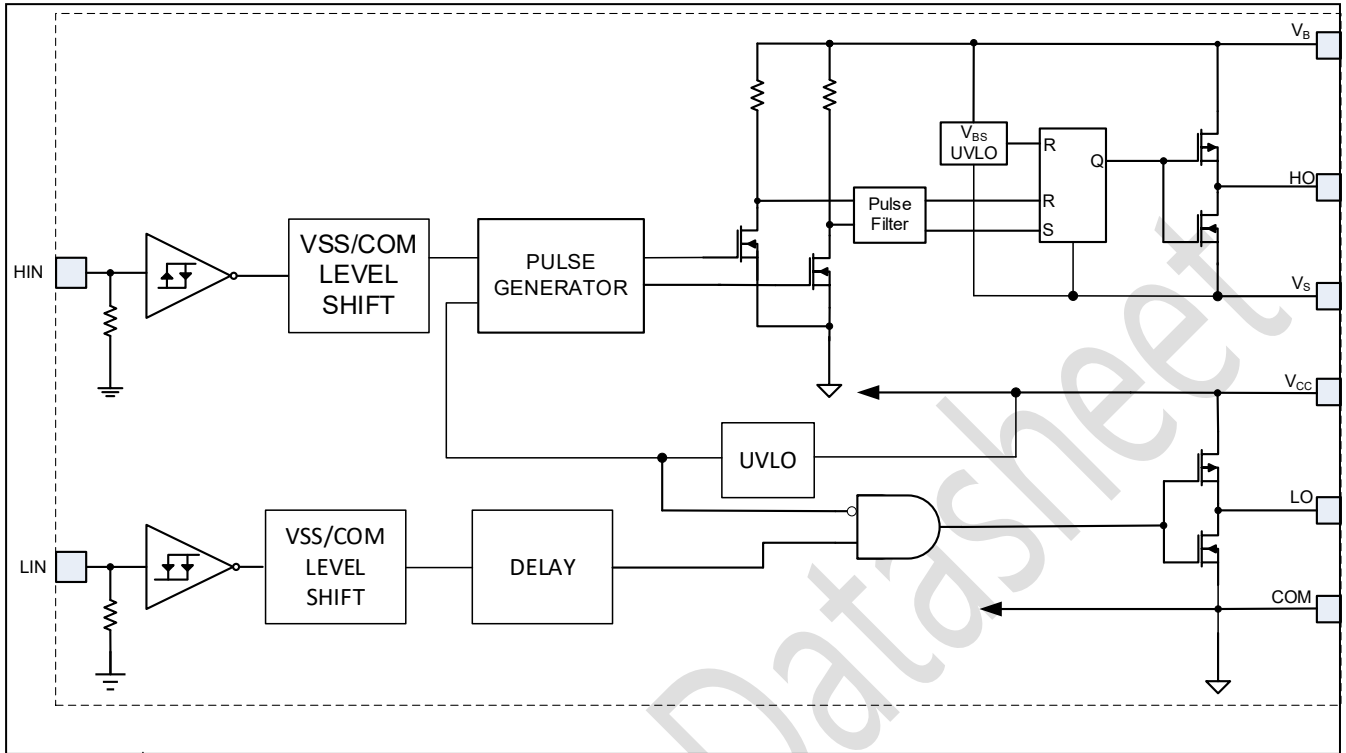
Package	Pin Configuration (Top View)
SOIC-8	

**PIN DESCRIPTION**

No.	Pin	Description
1	V <sub>cc</sub>	Low-side and logic fixed supply
2	HIN	Logic input for high-side gate driver output (HO), in phase
3	LIN	Logic input for low-side gate driver output (LO), in phase
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V <sub>s</sub>	High-side floating supply return
7	HO	High-side gate drive output
8	V <sub>b</sub>	High-side floating supply

**ORDERING INFORMATION**
**Industrial Range: -40°C to +125°C**

Order Part No.	Package	QTY
SLM21867CA-DG	SOIC8, Pb-Free	2500/Reel
SLM21867CA-TG	SOIC8, Pb-Free	100/Tube

**FUNCTIONAL BLOCK DIAGRAM**

**SLM21867**

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Definition	Min.	Max.	Units	
V <sub>B</sub>	High-side floating absolute voltage	-0.3	625	V	
V <sub>S</sub>	High-side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3		
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3		
V <sub>CC</sub>	Low-side and logic fixed supply voltage	-0.3	25		
V <sub>LO</sub>	Low-side output voltage	-0.3	V <sub>CC</sub> + 0.3		
V <sub>IN</sub>	Logic input voltage (HIN & LIN )	-0.3	V <sub>CC</sub> + 0.3		
dV <sub>S</sub> /dt	Allowable offset supply voltage transient	---	50	V/ns	
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C	PDIP-8	---	1.0	W
		SOIC-8	---	0.625	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	PDIP-8	---	125	°C/W
		SOIC-8	---	200	
T <sub>J</sub>	Junction temperature	---	150	°C	
T <sub>S</sub>	Storage temperature	-55	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	---	300		

**Note:**

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High-side floating absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High-side floating supply offset voltage	Note 1	600	
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low-side and logic fixed supply voltage	10	20	
V <sub>LO</sub>	Low-side output voltage	0	V <sub>CC</sub>	
V <sub>IN</sub>	Logic input voltage (HIN & LIN)	COM	V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature	- 40	125	°C

**Note:**

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at a 15 V differential.

**DYNAMIC ELECTRICAL CHARACTERISTICS**
 $V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15\text{ V}$ ,  $C_L = 1000\text{ pF}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-on propagation delay	$V_S = 0\text{ V}$	---	170	250	Ns
$t_{off}$	Turn-off propagation delay	$V_S = 600\text{ V}$	---	170	250	
$t_r$	Turn-on rise time		---	22	38	
$t_f$	Turn-off fall time		---	18	30	
MT	Delay matching, HS & LS turn-on/off		---	---	35	

**STATIC ELECTRICAL CHARACTERISTICS**
 $V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15\text{ V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to COM and are applicable to all three logic input leads: HIN and LIN. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IH}$	Logic "1" input voltage	$V_{CC} = 7\text{ V to }20\text{ V}$	2.5	---	---	V
$V_{IL}$	Logic "0" input voltage		---	---	0.8	
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	$I_O = 20\text{ mA}$	---	---	1.4	
$V_{OL}$	Low level output voltage, $V_O$		---	0.02	0.15	
$I_{LK}$	Offset supply leakage current	$V_B = V_S = 600\text{ V}$	---	---	50	$\mu\text{A}$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	$V_{IN} = 0\text{ V or }5\text{ V}$	20	60	400	
$I_{QCC}$	Quiescent $V_{CC}$ supply current		200	290	400	
$I_{IN+}$	Logic "1" input bias current	$HIN=LIN = 5\text{ V}$	---	60	70	
$I_{IN-}$	Logic "0" input bias current	$HIN=LIN = 0\text{ V}$	---	---	5	
$V_{BSUV+}$	$V_{BS}$ supply undervoltage positive going threshold		5.65	6.25	6.85	V
$V_{BSUV-}$	$V_{BS}$ supply undervoltage negative going threshold		5.15	5.75	6.35	
$V_{CCUV+}$	$V_{CC}$ supply undervoltage positive going threshold		5.65	6.25	6.85	V
$V_{CCUV-}$	$V_{CC}$ supply undervoltage negative going threshold		5.15	5.75	6.35	
$I_{O+}$	Output high short circuit pulsed current	$V_O = 0\text{ V}$ $V_{IN} = \text{Logic "1"}$ $PW \leq 10\text{ }\mu\text{s}$	3.0	4.0		A
$I_{O-}$	Output low short circuit pulsed current	$V_O = 15\text{ V}$ $V_{IN} = \text{Logic "0"}$ $PW \leq 10\text{ }\mu\text{s}$	3.0	4.0		

### Switching and Timing Relationships

The relationships between the input and output signals of the SLM21867 are illustrated below in Figures 1, 2. From these figures, we can see the definitions of several timing parameters (i.e.,  $t_{ON}$ ,  $t_{OFF}$ ,  $t_R$ , and  $t_F$ ) associated with this device.

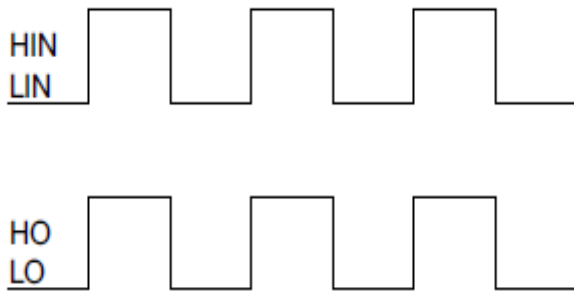


Figure 1. Input/Output Timing Diagram

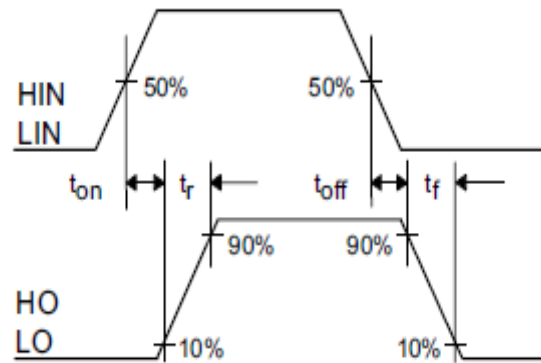


Figure 2. Switching Time Waveform Definitions

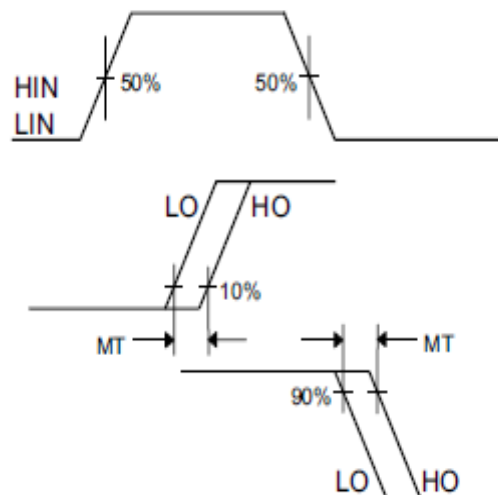
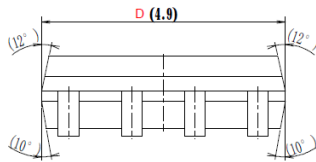
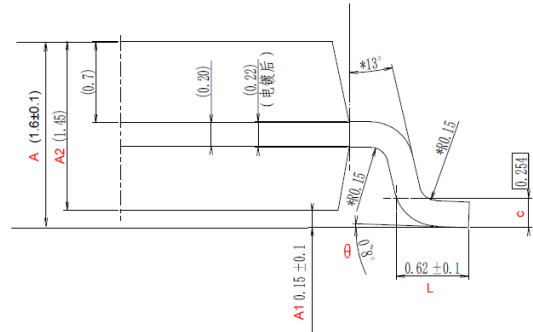
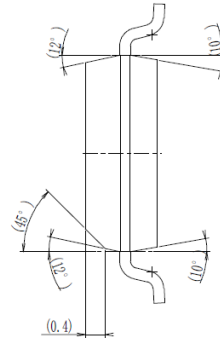
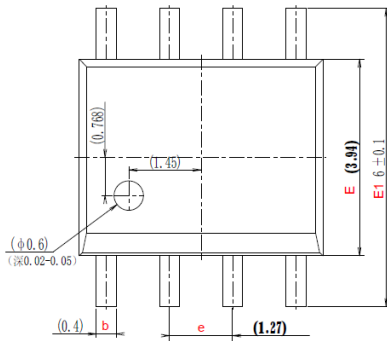
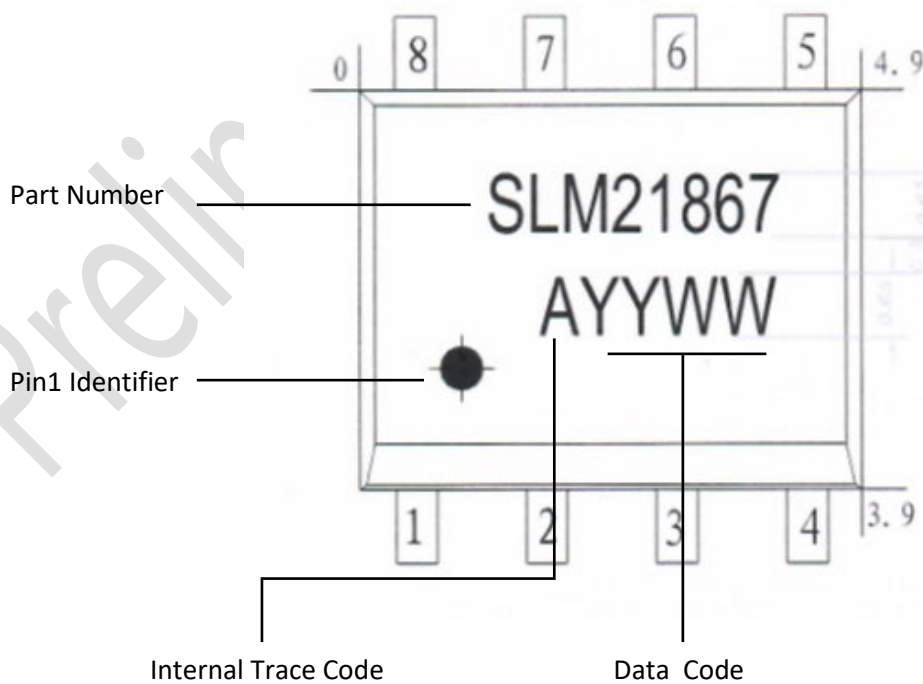


Figure 3. Delay Matching Waveform Definitions

**PACKAGE CASE OUTLINES**


字符	Dimension millimeters		
	Min	Standard	Max
A	1.500	1.600	1.700
A1	0.050	0.165	0.250
A2	1.350	1.450	1.550
b	0.300	0.400	0.500
c	0.220	0.254	0.280
D	4.800	4.900	5.000
E	3.840	3.940	4.040
E1	5.900	6.000	6.100
e	1.27 (BSC)		
L	0.520	0.620	0.720
θ	0°		8°

**PART MARKING INFORMATION**


## Revision History

Note: page numbers for previous revisions may differ from page numbers in current version

<b>Page or Item</b>	<b>Subjects (major changes since previous revision)</b>
<b>Rev 0.1 datasheet, 2019-9-1</b>	
Whole document	Draft datasheet released
<b>Rev 0.2 datasheet, 2020-1-14</b>	
Page 2	Change order information
Page 7	Add part marking information